ERURJ 2024, 3, 1, 804-815

(Original Article.)

Minimum Size Photonic Crystal OR Gate Structure

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Received 28th July 2023, Revised 22nd November 2023, Accepted 26th November 2023

DOI: 10.21608/erurj.2024.225738.1060

ABSTRACT

Photonic crystal applications and their high performance led them to be considered as a promising research area. The factors that affect their operation are the topology type, and the arrangement of its rod position, and their constructed materials. OR gate is proposed in this paper to be simulated and evaluated. This design is built on a square lattice- photonic crystal construction. Sensitivity analysis, and carefully rod locations are considered to obtain remarkable performance. Minimum size is the main property that distinguishes this design. Based on the simulations, a minimum size of 39.6 μm^2 is obtained. The bit rate of 3.2 Tb/s is calculated for this structure. The considered threshold power level is 0.25. Comparison table is well organized for the recently published photonic crystal OR-gate that is based on ring resonator topology. Finite difference time domain and plane wave expansion method are used to analyze the proposed structure at 1.55μm wavelength to verify OR- gate operation. The fabrication methods are discussed and evaluated. As will be shown the size is decreased by around 23% of the recently published paper.

Keywords: OR-gate; Photonic crystal applications; Ring resonator; Photonic crystal topology; Contrast ratio; Time response; Bit rate.

1. Introduction

New technologies are focused on miniaturizing circuit size, achieving high-speed data processing, and advancing digital computing. To accomplish this, electronic circuits are created using semiconductor materials [1, 2], with combinational and sequential logic designs used for different operations [3]. The need for high data rates has driven electronic devices to their limits, prompting the development of optical circuit models that can achieve high-speed applications with a small area. Examples of these models include semiconductor optical amplifiers (SOA) [4], periodically poled lithium niobate (PPLN) waveguides [5], and photonic crystal (Ph. Cs.) structures [3].

The speed of light has distinct advantages that make it a valuable component of photonic crystal (Ph. Cs.) technology, which offers a range of high-speed applications such as sensors [7], filters [8], logic gates (e.g. AND, OR, XOR) [9], multiplexers [10], demultiplexers [11], flip-flops [12], encoders [13], decoders [14], and half adders [15]. (Ph. Cs.) structures are artificial crystals made from highly ordered dielectric materials that consume less waste power [6].

By altering the topology of basic structures, a variety of applications can be created. These topologies are typically classified into ring resonator, self-collimation, waveguide, and cavity types. A recent paper [16] discusses the differences in characteristics between these topologies. Literature has shown that square and hexagonal lattices are commonly used [17, 18], and operation can be performed in both linear and nonlinear regimes. Software packages such as RSOFT [19] (which uses the finite difference time domain (FDTD) numerical technique) and COMSOL [20] (i.e., which mainly operate on the finite element method (FEM)) are used to simulate and analyze (Ph. Cs.) structures.

This article focuses on the examination and verification of two-dimensional (Ph. Cs.) OR gate ring resonator structures. Various figures of merit will be presented, including contrast ratio (CR), structure size, bit rate (BR), and linearity.

The paper is organized as follows: Section 2 provides details of the structure. Simulations and results are presented in Section 3. Section 4 contains some fabrication trends. The conclusions section comes in section 5, followed by a list of the most relevant references.

2. Basic Concepts

The OR gate is a fundamental digital logic block that consists of two inputs and one output. The output of the OR gate is high when at least one of its inputs is high, but it is low when both inputs are low. The Boolean expression and truth table for the OR gate are defined in Equation (1) and Table 1, respectively [3].

$$Q=A+B \qquad (1)$$

Table 1: OR- gate truth table

Input		Output
A	*B*	*OR*
0	0	0
0	1	1
1	0	1
1	1	1

3. Structure Description and Dimensions

The proposed minimum size photonic crystal OR gate structure is based on a two-dimensional (Ph. Cs.) square lattice with a lattice constant (a) of 0.6 µm, which is the distance between the centers of two rods. The structure consists of (10x11) Silicon (Si) rods in an air substrate, with a rod radius (r) of 0.12 µm and a refractive index (n) of 3.46. The design includes two inputs and one output, as shown in Figure 1. The core element of the design is a ring resonator, and one waveguide is used to guide the launched light from input (A). The location of the output ports is determined by sensitivity analysis to provide the best performance and output power response, which is superior to the shifted versions of the output ports.

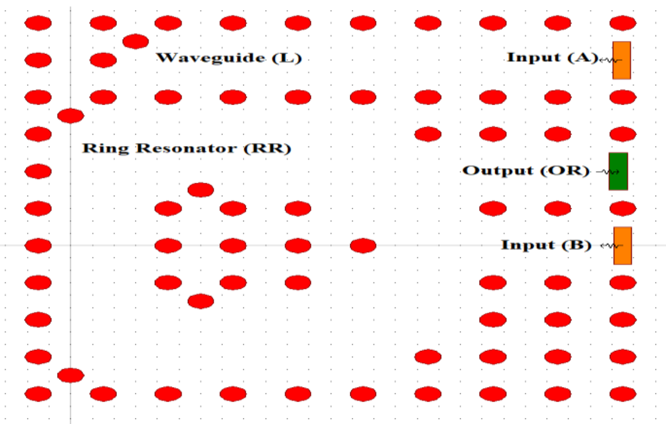

Figure 1: the proposed photonic crystal OR- gate structure

3. Simulation of the Proposed Gate

A. Numerical Methods and Photonic Band Gap (PBG) Range

Finite-difference time domain (FDTD) is a numerical method commonly used to simulate (Ph. Cs.) structures. This method provides information on power distribution, time response, and power level for each state. The photonic band gap (PBG), which is the range of forbidden optical frequencies that light cannot propagate, can be calculated using the plane wave expansion (PWE) method. In the simulation of the designs, the transverse electric (TE) field is applied.

According to Figure 2, the photonic band gap (PBG) range of the proposed structure is between 1.415 µm and 2.121 µm. The position of the input and output ports is determined using sensitivity analysis, as shown in Figure 1. The ring resonator topology is carefully designed to operate within the C-band optical wavelength range, which is between 1530 and 1565 nm.

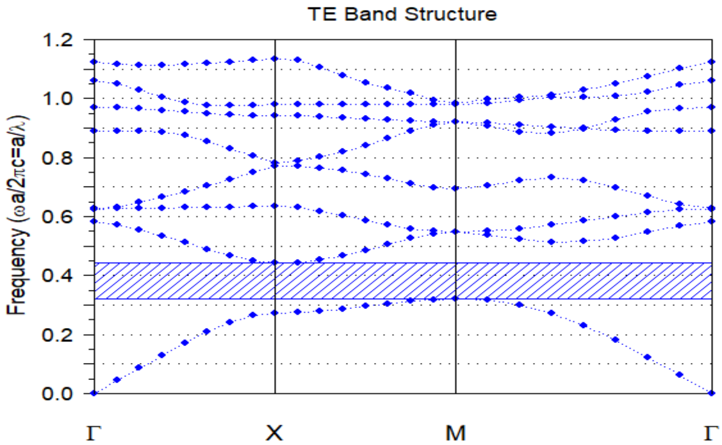

Figure 2: the photonic band gap (PBG) of TE- polarization

B. The Proposed OR Gate Operation

This section investigates the power distribution and time response of the proposed structure at a wavelength of 1.55 µm. Four states are examined to verify the operation and extract valuable results. The output power levels are normalized, and as shown in Figure 1, the output is switched on and off based on the state of the two inputs, as explained in the following section.

1) Case 1: If no power is applied to both inputs, the output port will have no power.

2) Case 2: If one of the inputs is on (i.e., input A=1, B=0), a light wave will travel through the waveguide and mutually couple into the ring resonator. The power in the ring resonator is then guided by the scattering rods to reach the output. Figure 3 illustrates this state, with the output equal to 0.28, which is considered logic (1).

3) Case 3: On the other hand, when power is launched through port B (i.e., B=1) and the other port is disabled (i.e., A=0), the signal circulates within the ring at its resonant wavelength of 1.55 µm, delivering power directly to the output port. The output is logic (1) with a power level of 0.3, as shown in Figure 4.

4) Case 4: When both inputs (i.e., A and B) are logic (1), a field is constructed between the two input beams, as shown in Figure 5. The output in this case is equal to 0.55, confirming the OR-gate operation.

C. Bit Rate (BR) calculation

The bit rate is defined as the reciprocal of the response time (RT) as show in equation (2) [9].

$$RT = t_d + t_r + t_f = t_d + 2t_r \quad (2)$$

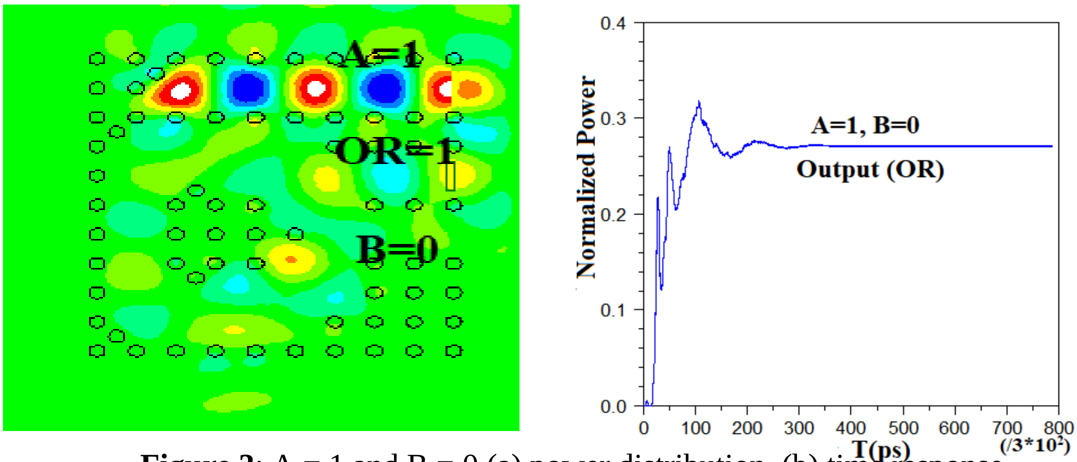

Figure 3: A = 1 and B = 0 (a) power distribution, (b) time response.

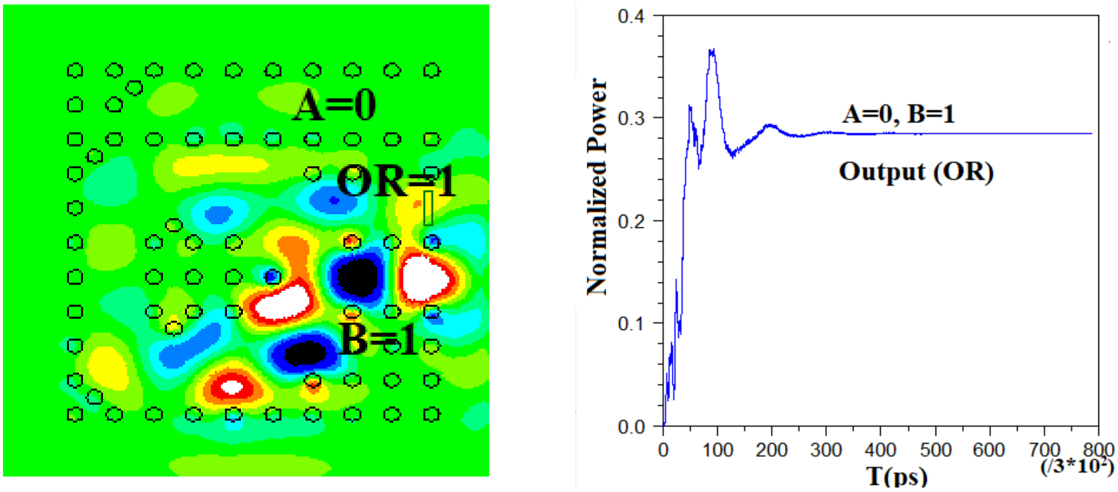

Figure 4: A = 0 and B = 1 (a) power distribution, (b) time response.

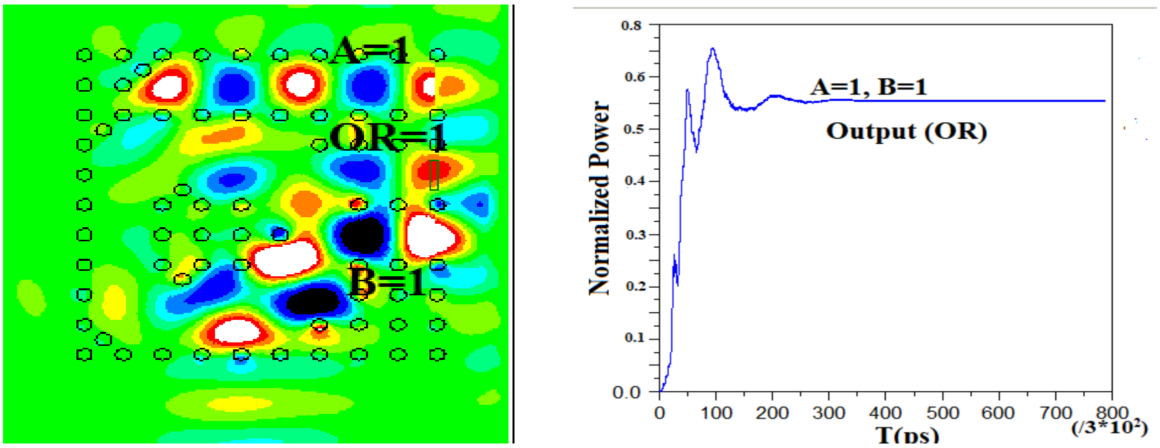

Figure 5: A = 1 and B = 1 (a) power distribution, (b) time response

The delay time (t_d) is defined as the time it takes for the output power to rise from 0 to 10% of the steady-state output power. The transition time (t_r) is the time taken for the output power to go from 10% to 90% of the average output power. The falling time (t_f) is the time it takes for the final steady-state power to drop from 90% to 10%, which is approximately equal to the transition time (t_r) in linear material scenarios, as in [9]. The bit rate (BR) is calculated from the time response to be 3.2 Tp/s.

Table 3 provides a comparison between the proposed structure and its counterparts in the literature. Most of the designs use Silicon (Si) as the rod material. The maximum number of gates is reported in [27], while the maximum size of 1287 μm^2 is reported in [30]. The highest contrast ratio (CR) is reported in [31] for a hexagonal lattice type with only OR-gates, as shown in Table 3. The proposed structure for the OR-gate has a minimum size and is compatible with the bit rate (BR). It can be implemented with the same rod radius and does not require any auxiliary inputs to verify its operation.

Table 2: the power levels and the calculated bit rate for structure

Input		0- degree	
A	B	power	(BR) Tb/s
0	0	0	3.2
0	1	0.3	
1	0	0.28	
1	1	0.55	

Table 3: comparison between the published all- optical OR- gate ring resonator based in the literature

Ref. and Year	Contrast ratio (dB)	Bit rate (Tb/s)	Size (μm^2)	Auxiliary input	Implemented gates
Ref [21-2015]	16.7	0.33	136	√	OR, AND, XOR
Ref [22-2015]	4.77	0.2	303	√	OR, AND, XOR, NOT
Ref [23-2015]	18.7	0.33	499	√	OR, NOT
Ref [24-2016]	NA	0.8	200	X	OR
Ref [25-2017]	NA	0.33	134	X	OR, AND
Ref [26-2017]	25	0.13	283	√	OR, NOR
Ref [27-2017]	NA	3.8	132	X	OR, AND, XOR, NOT, NOR, NAND, XNOR
Ref [28-2018]	9.29	NA	335	√	OR, AND, NAND
Ref [29-2019]	18	4.7	250	√	OR, AND
Ref [30-2019]	19	0.5	1287	√	OR
Ref [31-2021]	29	5	454	√	OR
Ref [32-2022]	NA	2.5	56.2	X	OR
Ref [33-2022]	NA	5.02	56.16	X	OR, XOR, NOT
Ref [34-2023]	NA	1.35/6.35	51.48	X	OR
Proposed	**NA**	**3.2**	**39.6**	**X**	**OR**

4. Fabrication Trends

Till now the fabrication of (Ph. Cs.) applications face great challenges. Most of the proposed prototypes concentrate on laser sources [36], and sensors [37]. Electron beam or optical lithography combined with wet and dry etching [36], and ion beam drilling [37] are two types of the fabrication methods. These technologies reached to construct holes with radius 60 nm [38].

Most of the lithography methods suffer from its expensive machinery (i.e., as in optical mask method), or setup complexity (i.e., as in multi-holography method). On the other hand, Porous Anodic Alumina methods have some challenges such as: mold complex preparation (i.e., as in dot-like mold and nano imprint lithography), or angular precision and identical pressure applied (i.e., as in grating). So as shown the fabrication of (Ph. Cs.) applications still have some troubles to be solved.

5. Conclusion

This paper presents a new proposed design for an OR gate, which is implemented and analyzed for performance and figures of merit. The design operates in the linear regime, which helps to save power consumption. Two numerical techniques, FDTD and PWE methods, are used for simulation and analysis. The core element of this design is the ring resonator topology, and therefore, the comparison table is organized to focus on the same logic with this type of topology. The main objectives are to verify the OR logic gate and obtain the minimum size and compatible bit rate compared to other published papers in the literature. Future work will focus on studying the effect of temperature on such structures.

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